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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/624,627
Filing Date	July 21, 2003
First Named Inventor	Luan C. Tran
Art Unit	2811
Examiner Name	Jennifer Kennedy
Attorney Docket Number	MI22-2358

Total Number of Pages in This Submission

ENCLOSURES (*Check all that apply*)

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☑ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
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- ☐ After Allowance Communication to a Technology Center (TC)
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- ☐ Proprietary Information
- ☐ Status Letter
- ☑ Other Enclosure(s) (please Identify below):

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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual	Jennifer J. Taylor, Ph.D.; Reg. No. 48,711; Wells St. John P.S.
Signature	Jennifer J. Taylor
Date	November 11, 2003

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EL979950021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 10/624,627
Filing Date ..... July 21, 2003
Inventor ..... Luan C. Tran
Assignee ..... Micron Technology, Inc.
Group Art Unit 2811
priority Examiner ..... Kennedy, Jennifer J.
Attorney's Docket No. MI22-2358
Title: Methods of Forming Semiconductor Constructions

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References –See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR § 1.56. Copies of the cited art are included with the exception of U.S. patents and published U.S. applications (1276 OG 55). No admission is made regarding whether all the submitted references are prior art.

This Supplemental Information Disclosure Statement is being filed within three months of the filing date of the application or before the mailing date of a first Office Action, whichever occurs last. Therefore, no fee is believed to be required. However, in the event that a fee is required for filing this Supplemental Information Disclosure Statement, please charge the fee specified under 37 C.F.R. § 1.17(p) to Deposit Account No. 23-0925.

Respectfully submitted,

Dated: November 11, 2003 By: Jennifer J. Taylor

Jennifer J. Taylor, Ph.D.
Reg. No. 48,711

EL979950021

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ATTY. DOCKET NO.	SERIAL NO.
MI22-2358	10/624,627
APPLICANT: Luan C. Tran	
FILING DATE: July 21, 2003	GROUP: 2811

U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	6,144,079 A	11-2000	Shirahata et al.			
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	AM	EP 0718881	06/96	EPO, Chan				
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		Watanabe, H. et al., *Novel 0.44μm² Ti-Salicide STI Cell Technology for High-Density NOR Flash Memories and High Performance Embedded Application*, IEEE 1998, pp. 36.2.1 - 36.2.4.
	AS		Wolf, S., "*Silicon Processing for the VLSI Era*", Vol. 2, pp. 632-635.
	AT		MITSUBISHI ELECTRIC WEBSITE: Reprinted from website http://www.mitsubishielectric.com/r_and_d/tech_showcase/ts8.php on 3/29/2001: "*8. Production Line Application of a Fine Hole Pattern-Formation Technology for Semiconductors*", on 3/29/2001, 4 pgs

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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		FILING DATE July 21, 2003	GROUP 2811

U.S. PATENT DOCUMENTS

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	AB	5,635,744	06-1997	Hidaka et al.			
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	AR		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from http://www.semiconductor.net/semiconductor/issues /1999/sep99/docs/feature1.asp on 3/29/2001: "*Resists Join the Sub-λ Revolution*", 9 pgs.
	AS		CAHNERS SEMICONDUCTOR INTERNATIONAL WEBSITE: Reprinted from http://www.semiconductor.net/semiconductor/issues/1999/aug99/docs/lithography.asp on 3/29/2001: "*Paths to Smaller Features*", 1 pg.
	AT		Wolf, S., "*Silicon Processing for the VLSI Era, Vol. 1: Process Technology,*" Lattice Press 1986, pp. 434-437.

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	AC	US2002/0182829A1	12-2002	Chen			
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	AF						
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	AH						
	AI						
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	AL						

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	AN							
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		*"Session 18: Integrated Circuits and Manufacturing - DRAM and Embedded DRAM Technology,"* 2001 IEDM Technical Program, 2001 IEEE International Electron Devices Meeting, Dec. 4, 2001, reprinted 11/15/01 from http://www.his.com/~iedm/techprogram/sessions/s18.html., pp. 1-2.
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	AT		

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